ABSTRACT

Electrostatic discharge (ESD) protection for circuits which utilize multiple power supply rails, both positive (Vdd) and negative (Vss). Vdd busses remain completely isolated, while Vss busses are joined by pairs of complementary polarity diodes (made typically with P+/N-well diodes in an N /P-substrate process) thus keeping Vss busses isolated from each other. The I/O diodes of high frequency I/O pads are arranged in a square layout to achieve the best current/capacitance ratio. Each pair of power rails is provided with its own power shunt circuit, placing each shunt in physical proximity to the I/O pad it must protect. Shunts are designed to clamp at a very low voltage during an ESD event using mostly PMOS transistors. The protection circuit is laid out such that the worst case ESD event will flow at most between two I/O pads and one power shunt.

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